FAN-OUT WAFER LEVEL EWLB TECHNOLOGY AS AN ADVANCED SYSTEM-IN-PACKAGE SOLUTION

Jacinta Aman Lim, Vinayak Pandey*, Aung Kyaw Oo**, Andy Yong**
STATS ChipPAC Inc., Fremont, CA, USA
*STATS ChipPAC Inc., Tempe AZ, USA
**STATS ChipPAC, Singapore
Jacinta.amanlim@statschippac.com

ABSTRACT
System-in-Package (SiP) technology continues to be essential for higher integration of functional blocks to meet the ever demanding market needs with respect to smaller form factor, lower cost and time to market. A typical SiP incorporates all or some form of Fan-Out Wafer Level packaging, wire bonding or flip chip that serves a multitude of applications such as optoelectronics, RF, power amplifiers, MEMS and application processors. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology which is achieved by redistributing bond pads onto mold compound has proven to shrink x, y and z dimensions of the overall SiP package. eWLB in combination with Package-on-Package (PoP) further enables higher integration of functional blocks such as silicon photonics with discrete passive components, logic and integrated passive devices (IPDs).

This paper will discuss the advantages of utilizing eWLB technology to create a SiP solution. We will review the design considerations for creating a double sided redistribution layer (RDL) on the bottom eWLB package with embedded discrete components. Board level reliability results for this package architecture will be examined. We will also review higher density requirements and the corresponding challenges for very fine line and space (5/5 or 2/2 um) whereby eWLB technology negates the need for an interposer and provides the ability to be directly attached to the substrate utilizing Copper (Cu) pillar post or lead free solder.

Key words: Fan Out System in Package, embedded Wafer Level BGA, double sided RDL, Integrated Passives

INTRODUCTION

The semiconductor industry is constantly faced with complex integration challenges as consumers want their electronics to be smaller, faster and higher performance with more and more functionality packed into a single device. The demand for these requirements has driven many new trends and innovations in advanced packaging technology. One of the solutions is System-in-Package (SiP). System-in-Package is a functional electronic system or sub-system that includes two or more heterogeneous semiconductor die (often from different technology nodes optimized for their individual functionalities), usually with passive components.

The physical form of the SiP is a module, and depending on the end application, the module could include a logic chip, memory, integrated passive devices (IPD), RF filters, sensors, heat sinks, antennas, connectors and/or power chip in packaged or bare die form.

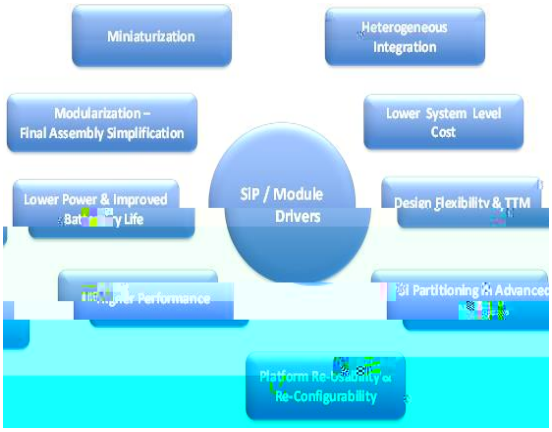


Figure 1. SiP/Module Drivers

This paradigm shift from chip scaling to system level scaling will continue to reinvent microelectronics packaging and [7]. The challenge of the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals rapidly.

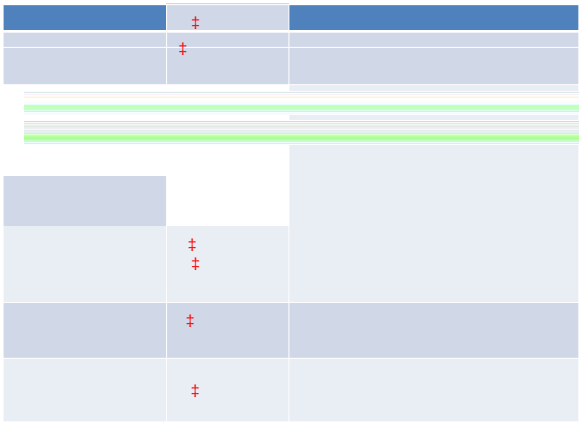
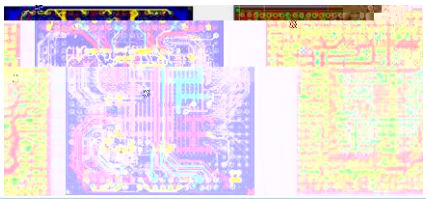


Figure 2. 2D SiP Technologies

To meet the above challenges, eWLB technology, also known as Fan-Out Wafer-Level Packaging (FOWLP), offers further form factor reduction and with the integration of passives and multi-embedded die capability, achieving more advanced 2D SiP configurations that are otherwise not feasible with laminate based flip chip (FC) or hybrid packa



Parameters	Laminate	eWLB	eWLB Improvement
Layer No.	4-L	2-L	50% reduction
[illegible]	[illegible]	60um staggered	Same
race W/S	20um/20um	10um/10um	50% reduction
[illegible]	60um/100 um (in prepreg/core)	25um	> 60% reduction
Pad	130um/200um	55um	>50% reduction
[illegible]	[illegible]	[illegible]	80% reduction

Figure 6. Case Study 2L eWLB Provides 2-3X Reduction in Area Relative to 4L Laminate

Functional test samples were prepared with a power management integrated circuit (PMIC) as shown in Figure 6. The SiP has a 6mm x 6mm body size with a 4mm x 4mm Si die and 12 discretes on the top. This eWLB SiP demonstrated more power efficiency performance compared to other embedded package technology and is representative of a significantly smaller package solution [5,7].

MEMS/Sensor eWLB

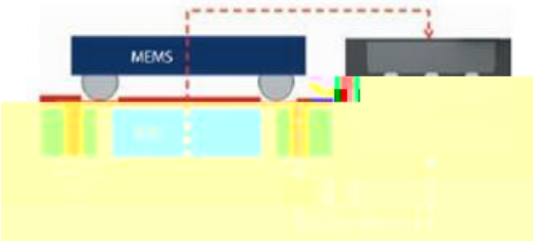


Figure 7. 3D eWLB for MEMS/Sensor Devices [2]

Figure 7 illustrates an eWLB sensor which has been miniaturized from the original side-by-side Land Grid Array (LGA) package. With a 3D vertical interconnection and multi-die stacking, it provides over 20% of a reduction in footprint and less than 1mm thickness with a lower cost high volume manufacturing (HVM) solution. The smaller body sizes (5mm/side or less) are typically a good fit for sensor devices such as health monitoring and environmental sensors.

Since sensor devices typically require at least a two chip solution (example ASIC and MEMS/Sensing silicon), advanced Fan-out eWLB stack-up solutions can enable a very small pitch LGA and ball grid array (BGA) eWLB PoP footprint at a competitive cost vs. the incumbent wire bond solutions. The package architecture enables routing on both sides of the package by embedding a direct via across the top to pad side of the package. The top MEMS device is bumped through standard lead frame wafer processing, singulated and assembled by pick and place tooling and reflowed on the ASIC in the eWLB bottom package. This assembly will eliminate the need for die attach material, assembly wires, protective glob-top and also the typical metal cap or molded package with access cavity, thus removing the typical laminate or leadframe for routing. Consequently, 3D eWLB SiP offers a much smaller footprint, simplified bill of material and can be assembled with a cost competitive panel level manufacturing process [7,10].

Double Sided RDL eWLB for Antenna in Package

The requirement for SiP integration is a growing trend for advanced application processors, RF, MEMS and Sensors in wearable electronics as a way to cost effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor. One example of growing demand for eWLB SiP is Antenna in Package applications which require advanced integration and miniaturization capabilities.

Figure 8 shows an example of SiP eWLB 2 layer RDL Antenna-in-Package module. The antenna is created on the bottom side of the eWLB package and antenna ground plane is created on the top side of the eWLB with RDL. Electrical connection from top to bottom of the eWLB package is created via printed circuit board (PCB) Copper bars.

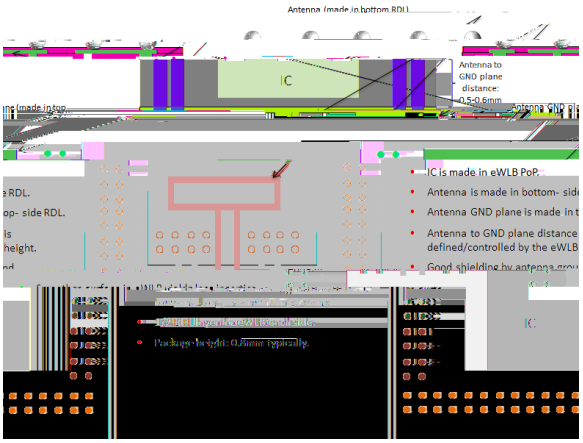


Figure 8. Double Sided RDL eWLB AiP Module

Integrated Passives in eWLB-SiP

In GSM, WCDMA, and EDGE mobile applications, many functional blocks such as power amplifiers (PA), baluns, transceiver, filters, etc., play a key role in performance of the module. Even though PAs are typically made from Gallium Arsenide (GaAs) due to its good electrical and thermal properties, they are quite expensive. In an RF circuit, a power amplifier has an impedance matching circuit consisting of capacitors and inductors which consume significant portion of the die size. This can potentially be replaced by an IPD and successfully used for RF modules/SiP in PA impedance matching and coupling circuits [8].

For this PA module, a multi-chip eWLB has been developed with PA and IPD integrated in a side-by-side configuration.

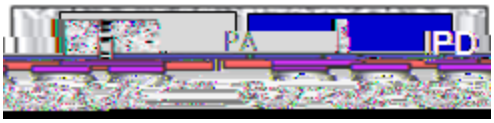


Figure 9. Side View of PA and IPD in SIP

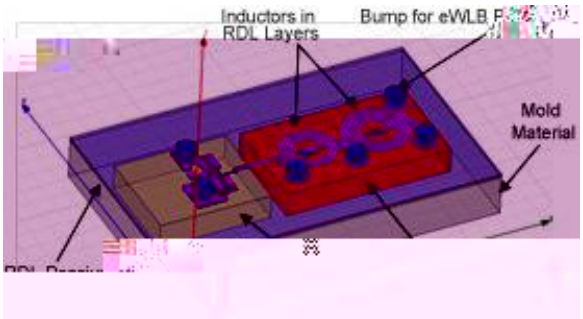


Figure 10. Illustration of a PA Die and Silicon IPD Die Embedded in Mold Substrate

Figures 9 and 10 illustrate an eWLB package which includes a PA chip and an IPD chip. The IPD die mainly serves as impedance matching network for the PA.

In this multi-die eWLB package the connection from the RDL to the PA chip is made through the via connecting the RDL layer and the top metal layer in the PA chip.. There are three different substrates used in this package; CMOS substrate, IPD substrate and mold compound substrate as shown in Figure 10. The passivation and redistribution layers are fabricated through a standard thin film process and plating in a wafer fabrication process, thus forming a multi-die eWLB package after standard backend processes.

2/2um Line Width and Spacing (LW/LS) with 3-Layer RDL [2]

In wafer level designs, the I/O pads are often placed in an uneven distribution. Therefore, RDL is required to connect these pads to the ball. From package to board, a similar redistribution is also needed for the signal array to escape outward to other devices.

Figure 11. SEM Image of 5/5um and 2/2um LW/LS RDL

A multi die eWLB 3 layer RDL test vehicle was designed with 2/2um, 5/5um and 10/10um line width/spacing (

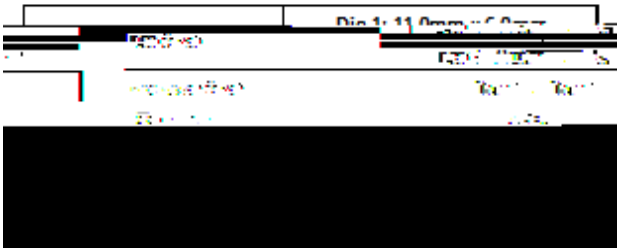


Table 1. Attributes of Test Vehicle with 3L RDL eWLB

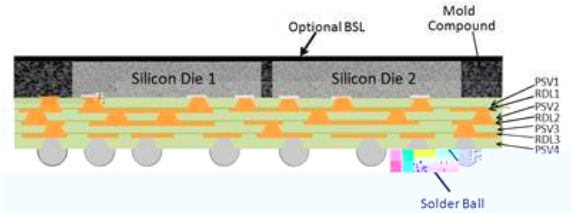


Figure 12a. Multi Die eWLB with 3L RDL Cross Section

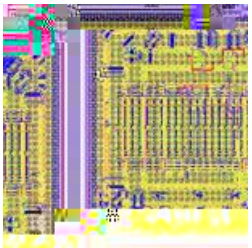


Figure 12b. 3-Layer RDL Design Layout of Test Vehicle

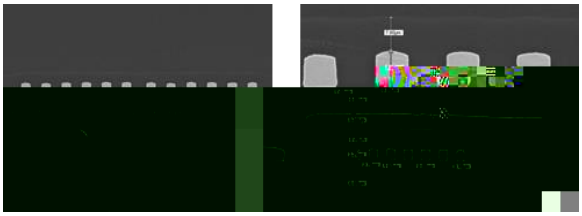


Figure 12c. SEM image of 3-Layer RDL eWLB Test Vehicle

Side by side multi-chip packaging can provide more design flexibility for SiP applications because a chip designer has more freedom in pad location as well as circuit block allocation. The fine pitch metal line width and spacing capabilities as well as multi-layer RDL process that utilizes a wafer fab photolithography process enables eWLB to provide a greater advantage over conventional flip chip technology with better electrical performance.

RELIABILITY TEST RESULTS

Leakage Current Test

Leakage Current Test is used to measure the undesirable leakage current that flows through or across the surface of the insulation of the dielectric of a capacitor. This test is used to help ensure that the processes and assembly practices are satisfactory and reliable.

For 2/2um and 5/5um LW/LS test vehicle, leakage current

was measured as shown Table 2. It shows quite robust leakage current performance for both packages.

Table